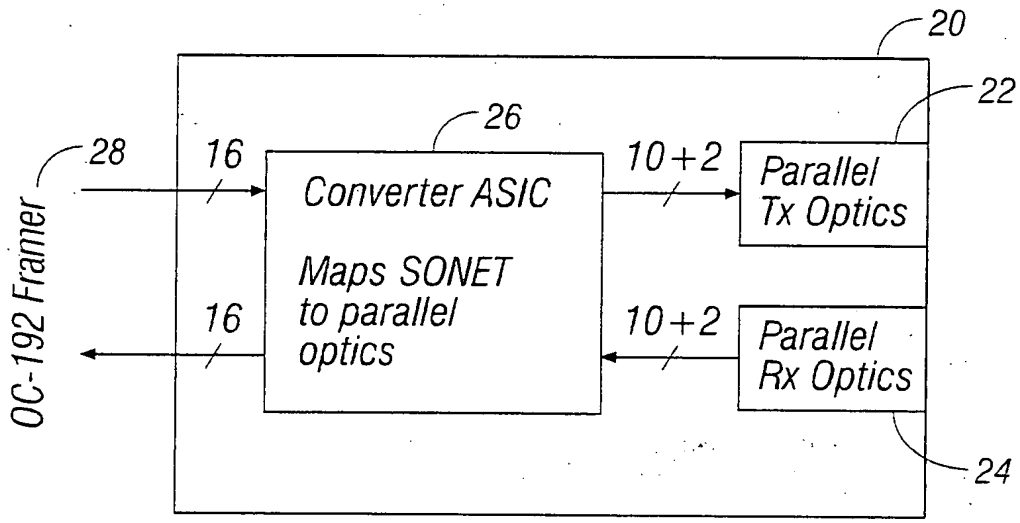


FIG. 1

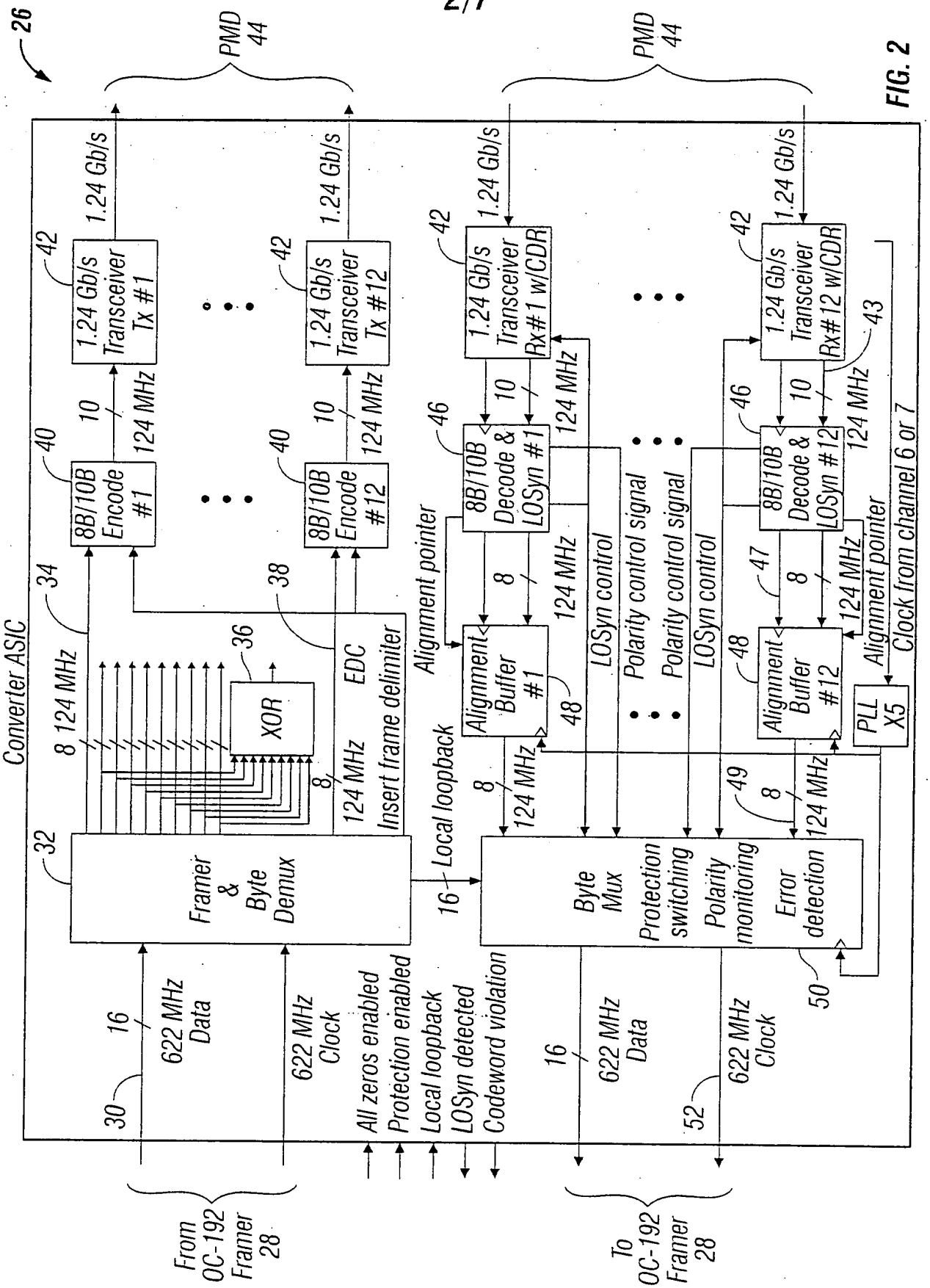

26
Converter ASIC
PMD 44
PMD 44
1.24 Gb/s
1.24 Gb/s Transceiver Tx #1
1.24 Gb/s Transceiver Tx #12
1.24 Gb/s Transceiver Rx#1 w/CDR
1.24 Gb/s Transceiver Rx#12 w/CDR
8B/10B Encode #1
8B/10B Encode #12
8B/10B Decode & LOSyn #1
8B/10B Decode & LOSyn #12
10
124 MHz
8 124 MHz
XOR
EDC
Insert frame delimiter
Alignment pointer
Alignment Buffer #1
Alignment Buffer #12
8
124 MHz
LOSyn control
Polarity control signal
Framer & Byte Demux
Local loopback
Byte Mux
Protection switching
Polarity monitoring
Error detection
PLL X5
Clock from channel 6 or 7
16
622 MHz Data
622 MHz Clock
All zeros enabled
Protection enabled
Local loopback
LOSyn detected
Codeword violation
From OC-192 Framer 28
To OC-192 Framer 28
30
32
34
36
38
40
42
43
46
47
48
49
50
52

FIG. 2

Code group name	Octet Value	Current RD- abcdei fghj	Current RD+ abcdei fghj
K28.5	BC	001111 1010	110000 0101
D3.1[a]	23	110001 1001	110001 1001
D21.2[a]	55	101010 0101	101010 0101

a. Both D3.1 and D21.2 have neutral mark/space density.

FIG. 3

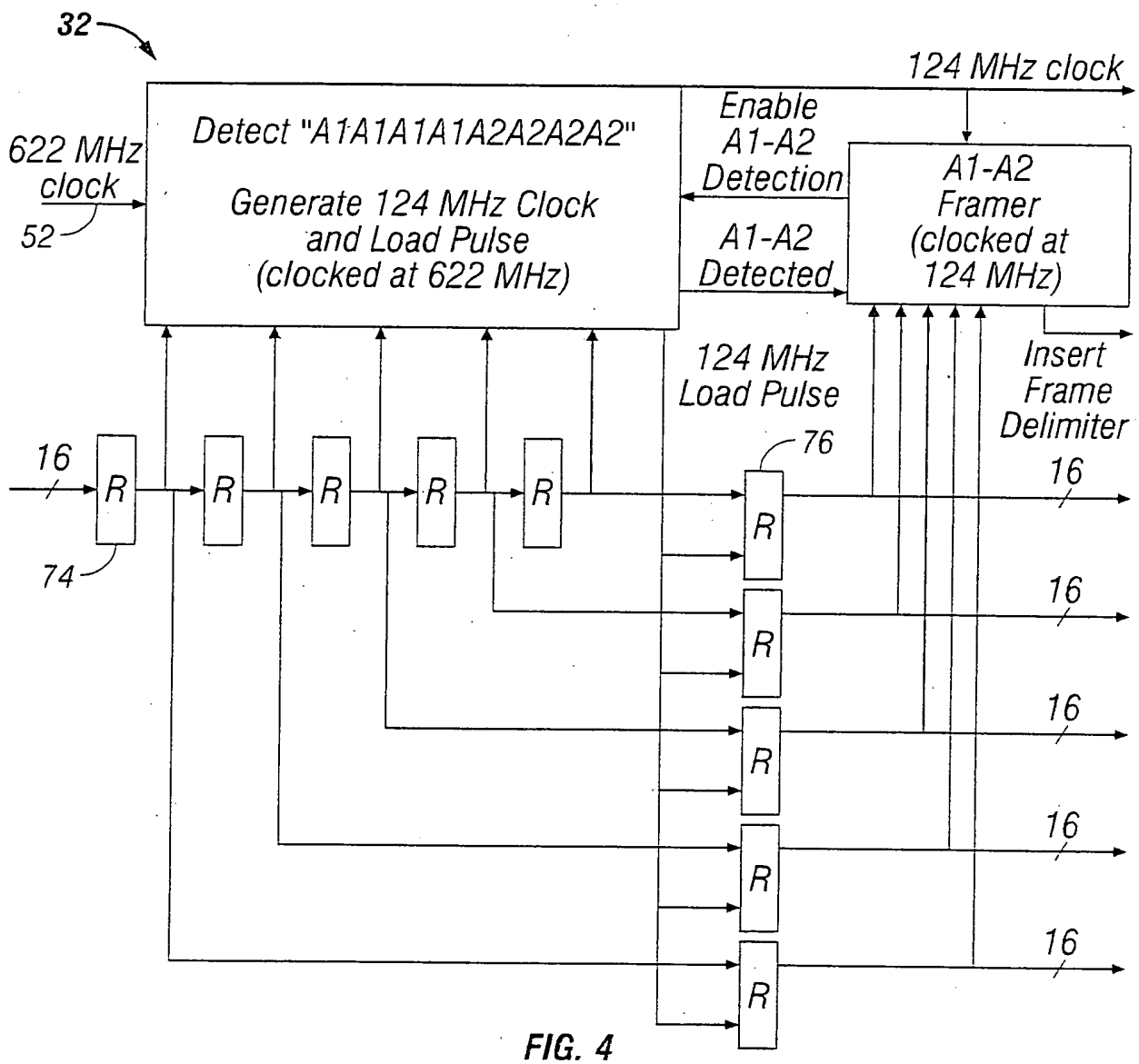


FIG. 4

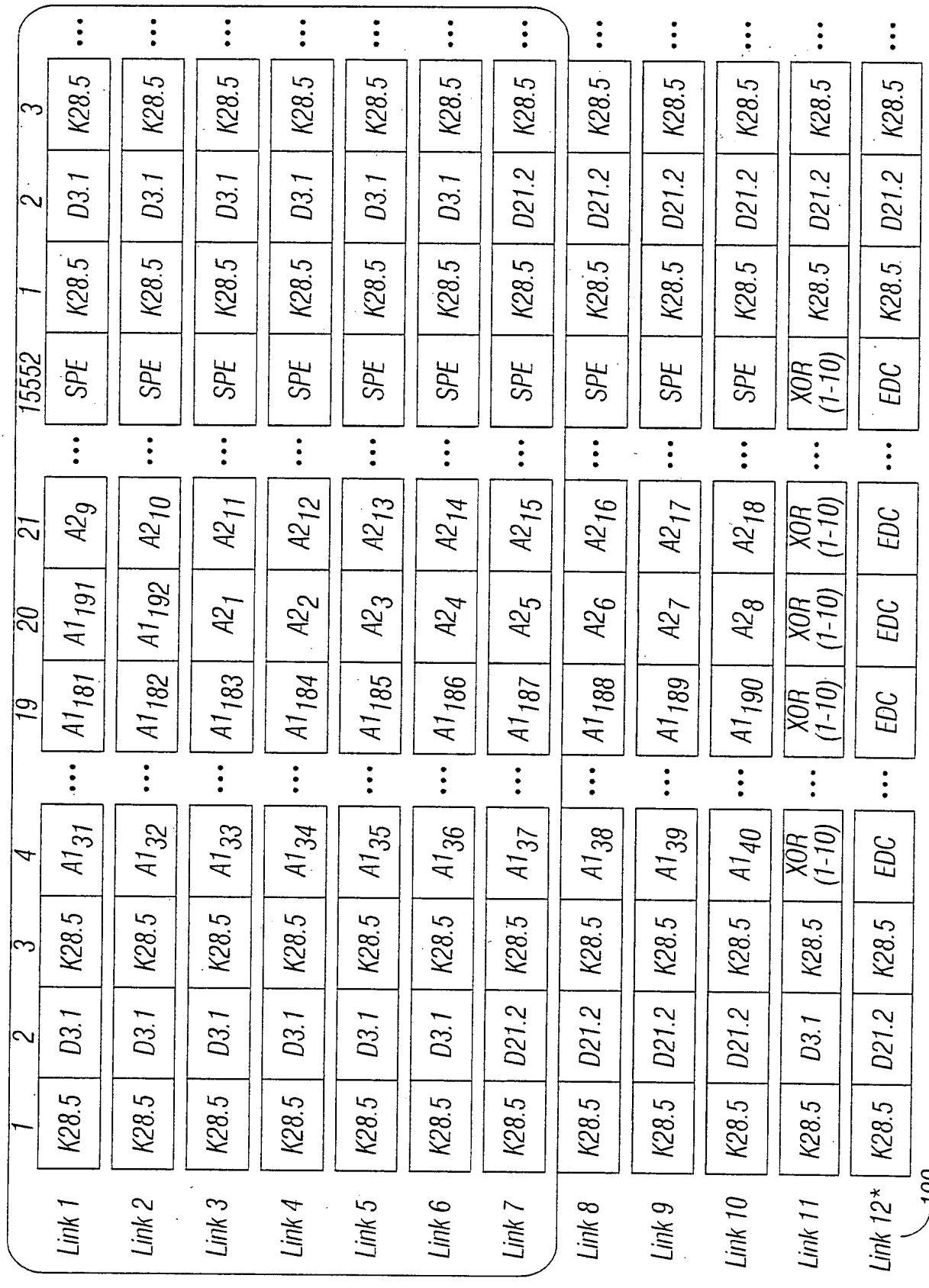

1
2
3
4
19
20
21
15552
1
2
3
Link 1
K28.5 D3.1 K28.5 A1_31 ... A1_181 A1_191 A2_9 ... SPE K28.5 D3.1 K28.5 ...
Link 2
K28.5 D3.1 K28.5 A1_32 ... A1_182 A1_192 A2_10 ... SPE K28.5 D3.1 K28.5 ...
Link 3
K28.5 D3.1 K28.5 A1_33 ... A1_183 A2_1 A2_11 ... SPE K28.5 D3.1 K28.5 ...
Link 4
K28.5 D3.1 K28.5 A1_34 ... A1_184 A2_2 A2_12 ... SPE K28.5 D3.1 K28.5 ...
Link 5
K28.5 D3.1 K28.5 A1_35 ... A1_185 A2_3 A2_13 ... SPE K28.5 D3.1 K28.5 ...
Link 6
K28.5 D3.1 K28.5 A1_36 ... A1_186 A2_4 A2_14 ... SPE K28.5 D3.1 K28.5 ...
Link 7
K28.5 D21.2 K28.5 A1_37 ... A1_187 A2_5 A2_15 ... SPE K28.5 D21.2 K28.5 ...
Link 8
K28.5 D21.2 K28.5 A1_38 ... A1_188 A2_6 A2_16 ... SPE K28.5 D21.2 K28.5 ...
Link 9
K28.5 D21.2 K28.5 A1_39 ... A1_189 A2_7 A2_17 ... SPE K28.5 D21.2 K28.5 ...
Link 10
K28.5 D21.2 K28.5 A1_40 ... A1_190 A2_8 A2_18 ... SPE K28.5 D21.2 K28.5 ...
Link 11
K28.5 D3.1 K28.5 XOR (1-10) ... XOR (1-10) XOR (1-10) XOR (1-10) ... XOR (1-10) K28.5 D21.2 K28.5 ...
Link 12*
K28.5 D21.2 K28.5 EDC ... EDC EDC EDC ... EDC K28.5 D21.2 K28.5 ...
100

FIG. 5

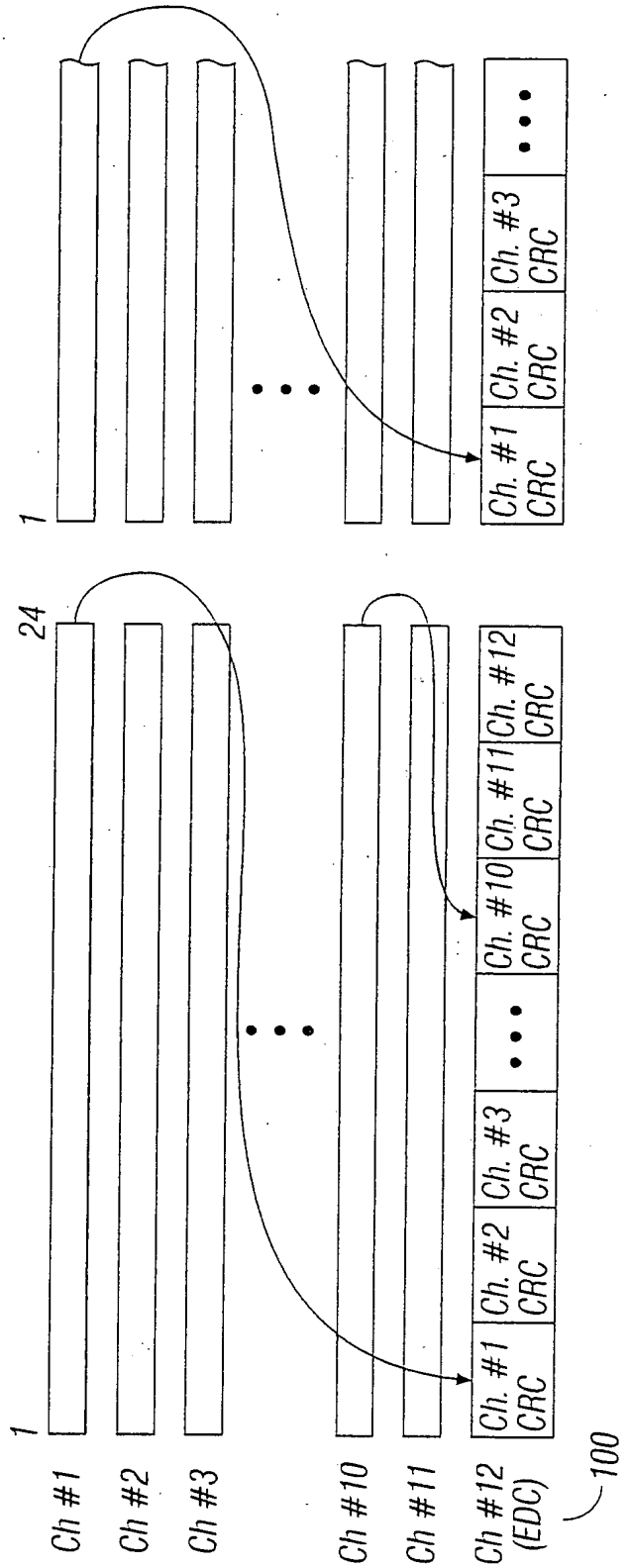

1
24
Ch. #1 CRC
Ch. #2 CRC
Ch. #3 CRC
Ch. #10 CRC
Ch. #11 CRC
Ch. #12 CRC
Ch #1
Ch #2
Ch #3
Ch #10
Ch #11
Ch #12 (EDC)
100

FIG. 6

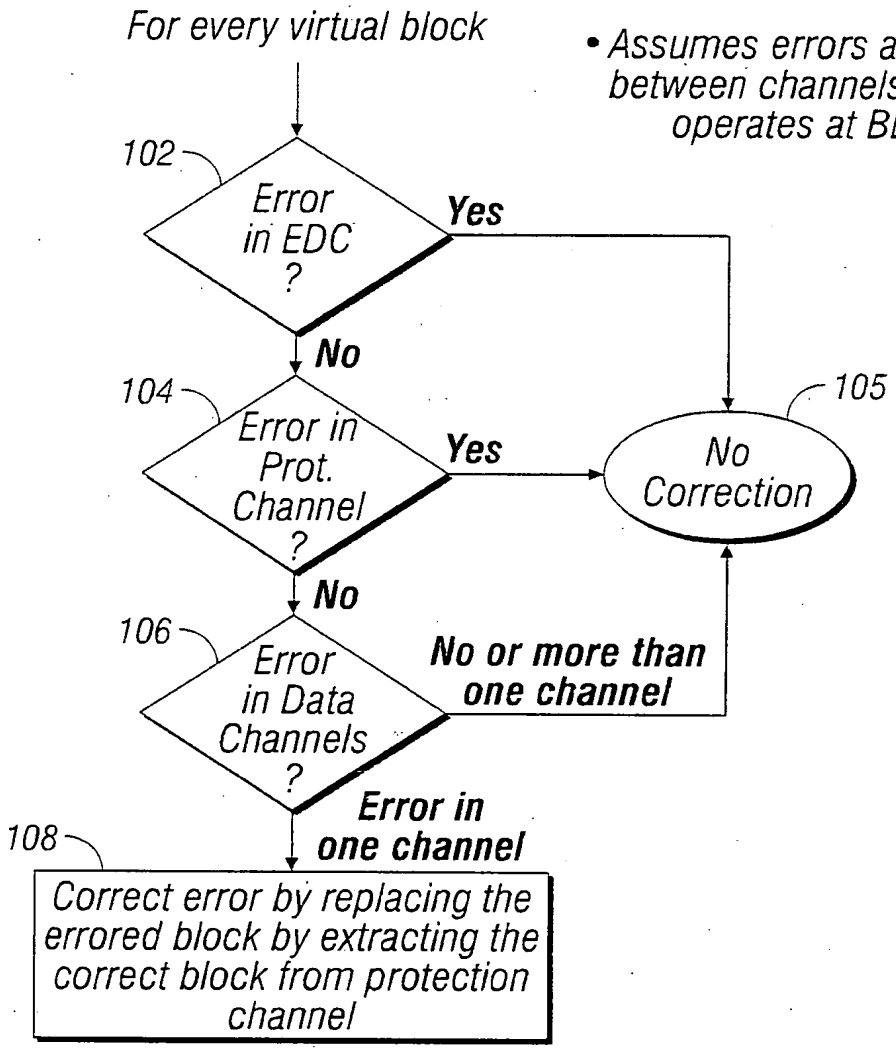

For every virtual block
• Assumes errors are uncorrelated between channels (each channel operates at BER <10-12)
102
Error in EDC ?
Yes
No
104
Error in Prot. Channel ?
Yes
105
No Correction
No
106
Error in Data Channels ?
No or more than one channel
Error in one channel
108
Correct error by replacing the errored block by extracting the correct block from protection channel

FIG. 7

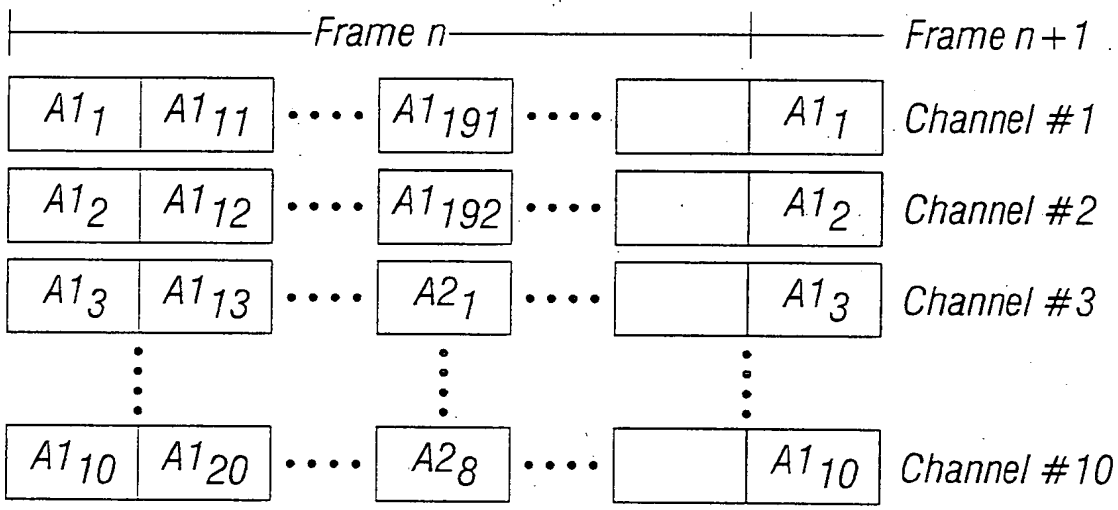
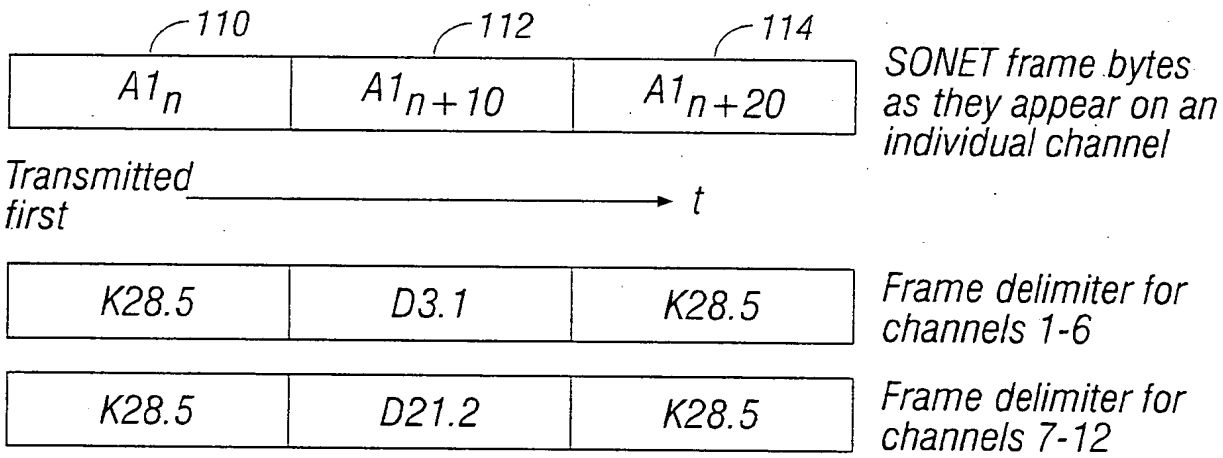


FIG. 8



Note: D3.1 and D21.2 have neutral running disparity to ensure that two K28.5's have opposite disparity.
D3.1 and D21.2 are used as the channel identifiers

FIG. 9